Remarks:

Reconsideration of the application is requested.

Claims 1-9 remain in the application.

In the third paragraph on page 2 of the above-identified Office action, the Examiner stated that the title of the invention is not descriptive. The Examiner further stated that a new title is required that is clearly indicative of invention to which the claims are directed. The title has been amended so as to facilitate prosecution of the application.

In the first paragraph on page 3 of the Office action, clai 1-3; and 5-9 have been rejected as being obvious over Leung al. (U.S Patent No. 5,563,762) in view of Matsuoka et al. (Patent No. 6,130,449) under 35 U.S.C. § 103.

In the second paragraph on page 4 of the Office action, cla 4 has been rejected as being obvious over Leung et al. (U.S Patent No. 5,563,762) in view of Matsuoka et al. (U.S Paten No. 6,130,449) and in further view of Kuroiwa et al (U.S Patent No. 6,239,460 B1) under 35 U.S.C. § 103.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form a the claims have, therefore, not been amended to overcome th references.

Before discussing the prior art in detail, it is believed t a brief review of the invention as claimed, would be helpfu

Claim 1 calls for, inter alia:

"an insulation layer covering said contact area and said memory element and having at least one opening formed there and leading to said contact area; and

an electrically conductive material filling said opening fo making contact with said second metal layer."

The Leung et al. reference discloses a capacitor for an integrated circuit which is placed on top of the passivatio layer of an otherwise complete integrated circuit (IC), as close to the end of processing as possible (column 3, lines 46-49). Furthermore, fabrication of the interconnect metallization for sub-micron integrated circuits typically includes one or more planarization steps to maintain planar for each interconnect level, and thus provides a top surfac having a flat passivation layer. This planar surface of th

passivation layer provides an ideal place to build capacitc (column 3, lines 49-54).

The Leung et al. reference further teaches that it seeks to avoid or reduce the problems mentioned in connection with t conventional prior art (column 3, lines 27-31), which place the capacitor underneath the metallization layers (column 2 lines 27-56; Figs. 1 and 2). The problems are as follows: contamination of active devices by the ferroelectric materi (column 2, lines 57-61); subjecting the capacitor to ion bombarding during subsequent processing (column 2, lines 57 67); reducing the porosity of the interconnect routing, i.e the interconnect must be routed around rather than through relatively large area occupied by the capacitor (column 3, lines 1-7); and stress related fatigue of the ferroelectric material (column 3, lines 8-14).

In the Leung et al. reference the solution to the above-mentioned problems is directly connected with the formation the capacitor **on top of the integrated circuit.** It is stat in column 4, lines 43-35 that "the capacitor structure is particularly beneficial in reducing device contamination concerns by physically separating ferroelectric capacitors from the active device". Further it is stated that "it is necessary to re-rout interconnect and contacts to the underlying devices" (column 3, lines 65-66). The reference

also teaches that due to the processing of the ferroelectri material after completion of the underlying IC, degradation the ferroelectric material is reduced or avoided (column 4, lines 50-53).

In the Leung et al. reference all of the preferred embodime show a capacitor on top of the integrated circuit. In Fig. the capacitor is placed on a top dielectric layer (114), wh has bond pad openings (118). Clearly, bond pad openings ar only formed within the top-level metallization layer. The same applies for the second embodiment (Fig. 4). For detai please refer to the Fig. 3 shown below.

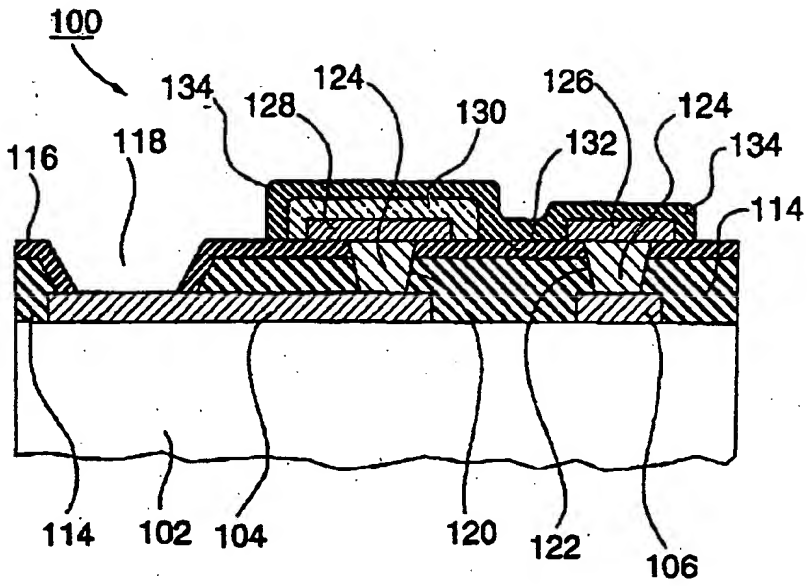

FIG. 3

The Matsuoka et al. reference discloses a semiconductor mem having a capacitor integrated underneath a metallization la (15 and 1501) (Fig. 1).

The references do not show or suggest an insulation layer covering the contact area and the memory element and having least one opening formed therein and leading to the contact area; and an electrically conductive material filling the opening for making contact with the second metal layer, as recited in claim 1 of the instant application. According t the Leung et al. reference if covered, the capacitor should only be covered by a coating to provide scratch protection (column 4, lines 38-41). A further metallization (includin via formed within an opening in an insulating layer) coveri the capacitor is explicitly excluded by the Leung et al. reference. The Matsuoka et al. reference discloses a semiconductor memory having a capacitor integrated undernea a metallization layer. As stated above the Leung et al. reference discloses explicitly avoiding any metallization layer on top of the capacitor. Therefore, a person of ordinary skill in the art would not consider combining the teachings of Leung et al. and Matsuoka et al..

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, eith

show or suggest an insulation layer covering the contact ar and the memory element and having at least one opening form therein and leading to the contact area; and an electricall conductive material filling the opening for making contact with the second metal layer, as recited in claim 1 of the instant application. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent clai are ultimately dependent on claim 1, they are believed to b patentable as well.

Even though claim 1 is believed to be patentable further discussion of the dependent claims is given. Regarding the Kuroiwa et al. reference one can only take therefrom information regarding the formation of a standard capacitor A contact area for contacting the top electrode is not show

It seems that the Examiner considers two capacitors as one capacitor having a contact area. The Examiner deems the ri capacitor as a contact area (page 5, first paragraph of the Office action). It is the position of applicants that a person of ordinary skill in the art would not consider a separate capacitor as a contact area for the top electrode its neighboring capacitor.

Furthermore, a person of ordinary skill in the art would no take a modification, as claimed in claim 4 of the instant

application, into consideration. The Leung et al. referenc teaches to connect the top electrode from underneath. Therefore, it would require a conductive path from metallization layer (106) through via (122) and contact (12 to the top electrode (134) (Fig. 3 of Leung et al.). If on would leave a dielectric layer between the fourth and secon metal areas as claimed in claim 4 of the instant applicatio the conductive path would be interrupted by the interposed dielectric. An electrical connection of the top electrode would be impossible. Therefore, a person of ordinary skill the art would refrain from interposing the dielectric betwe the contact (126) and the top electrode (134) of Leung et a

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited.

In the event the Examiner should still find any of the clai to be unpatentable, counsel respectfully requests a telepho call so that, if possible, patentable language can be worke out.

Please charge any other fees which might be due with respec to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg P.A., No. 12-1099.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicant(s)

AKD:cgm

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Marked-up version of the specification:

Replace the title with the following: --Semiconductor Component Having a Material Reinforced Contact Area--